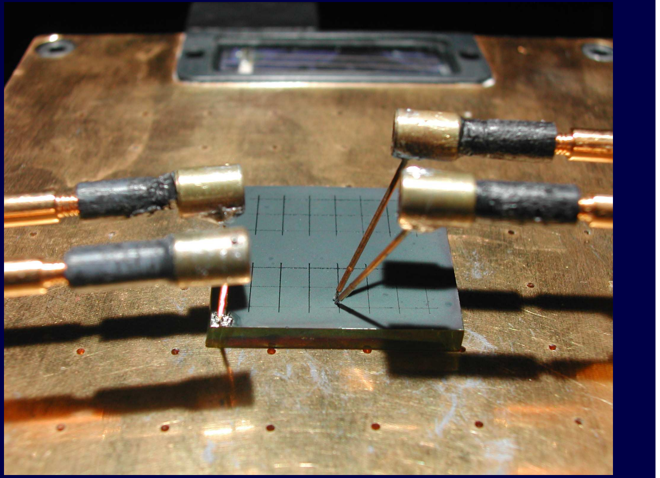
Les techniques microscopiques pour l'identification de l'origine de pertes de performance dans des cellules photovoltaïques à basse de CIS.



V. Bermúdez (1,3), C. M. Ruiz (1), E. Saucedo (3). V. Izquierdo (2), A. Pérez-Rodriguez (2)

(1) IRDEP, Institute de Recherche et Développement sur l'Energie Photovoltaïque (EDF R&D, CNRS, ENSCP), 6 Quai Watier, 78401 Chatou Cedex
(2) EME/CERMAE, Departament d'Electrònica, Universitat de Barcelona, C. Martí i Franquès 1, 08028 Barcelona, Spain
(3) NEXCIS, Z. I. 190, Av Celestin Coq, 13790 Rousset

outline

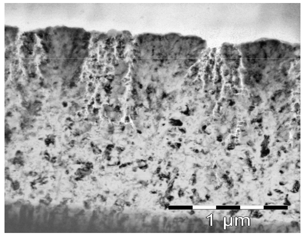
- CISEL et ses performances
- Electric problems identication
- Microscopy helping us to understand the situation

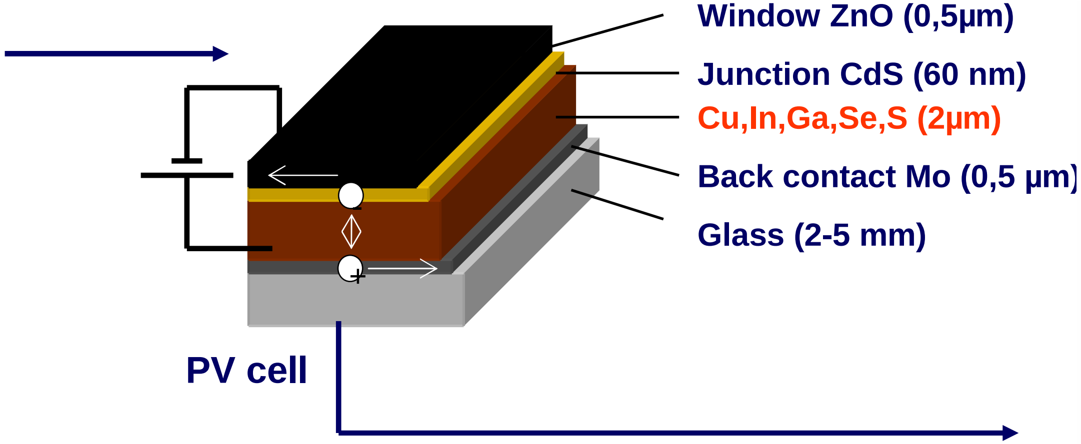
Who we are?

The CISEL^{TM} project, developed at IRDEP and transferred to NEXCIS, is based on the application of ED as cost effective method in order to replace vacuum based deposition processes for the synthesis of absorber layer

“CISEL” = CuIn(S,Se)$_2$ by Electrodeposition

ED *precursor*





PV cell

“Pre industrial” demonstrator

Focus on CISEL™ process

- CISEL™ has been developped by EDF R&D and CNRS-ENSCP (2003-2008)

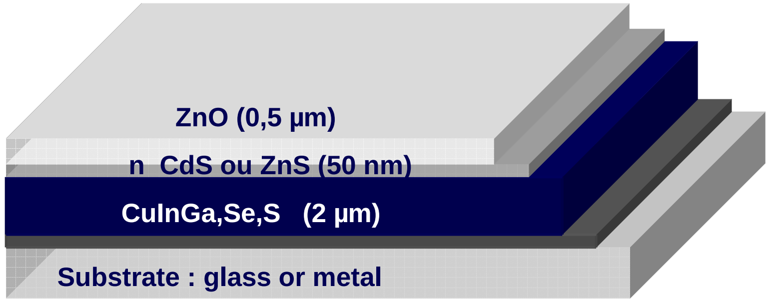
IRDEP INSTITUTE OF R&D ON PHOTOVOLTAIC ENERGY

CNRS CENTRE NATIONAL DE LA RECHERCHE SCIENTIFIQUE

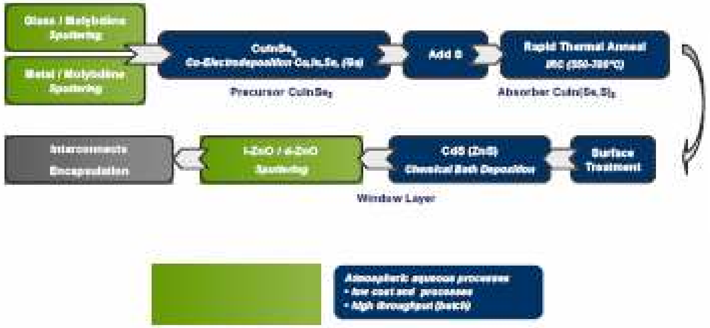
EDF R&D

ENSCP chimie paris

- CISEL™ is one of the Copper Indium Selenium and Gallium (CIGS) thin film technologies
- CISEL™ = wafer/modules
- 4 active layers



- CISEL™ is a 7 steps process
- CISEL™ process is similar to « chips » micro electronics process (including copper electrodeposition)
- CISEL™ is a low cost process, *i.e.* ≤ 0.70 €/wc module manufacturing cost



Cf slide 7

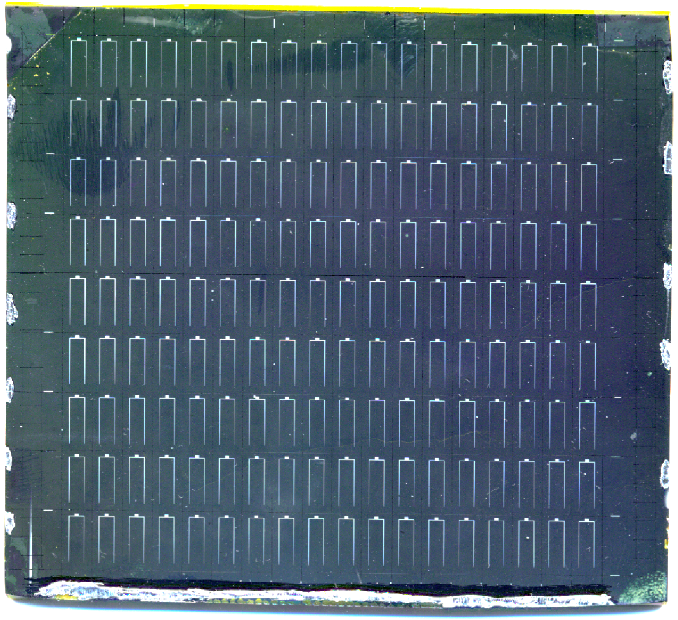
Highlights CISEL^{TM} PV performances*

With $CuIn(Se_{0.05}S_{0.95})_2$ absorber :

☑ 11,4 ±0.5% % on 0.1 cm^2 : record cell

☑ <8.5±0.5%> on 26 cm^2 : reproducible (<10%> can be achieved)

☑ <8%> on 30x30 cm^2 : record, **lack of homogeneity/reproducibility**



Material and optoelectronic diagnosis of process related losses

** measured by means of cartography of 0.1 cm^2 area cells without grid and without AR-coating*

State of the art & Roadmap CISEL™

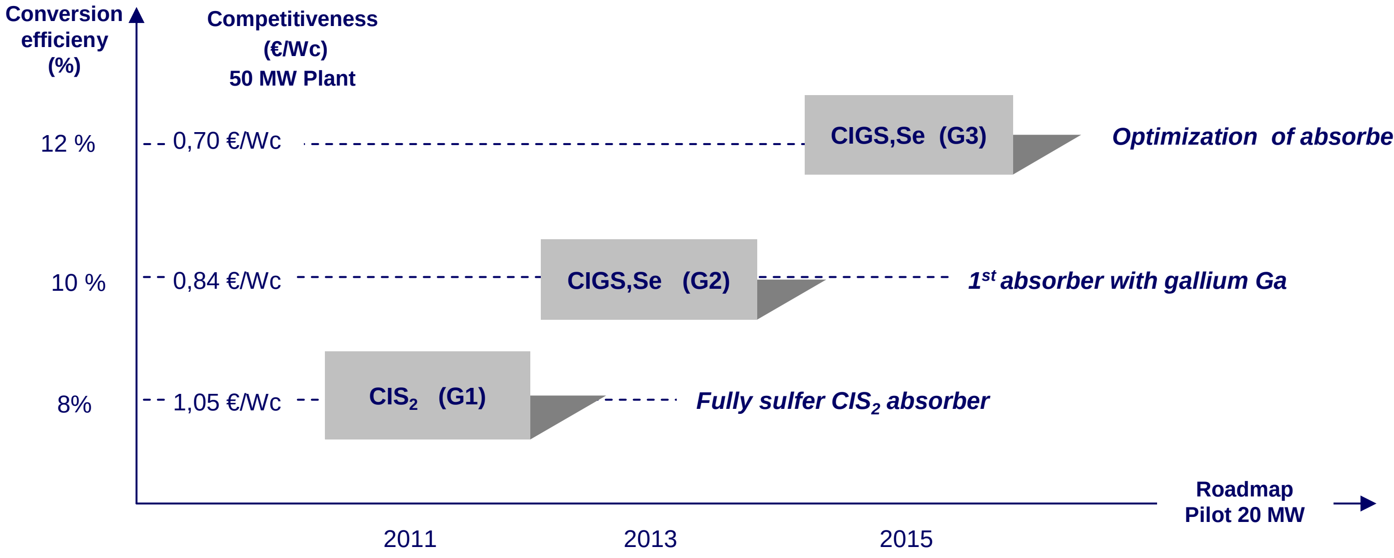
CISEL™ state of the art (IRDEP)

- **Proof of concept CISEL™ materials**
    - 11,4% 0,1 cm² cell (2004)
    - 10,5% 2 cm² mini-module (2005)
    - 8-9% 2,5x2,5 cm² wafer (2007)
    - 8% 15x15cm² wafers (2004)
- **Owned by EDF & CNRS: “at cost” issues**

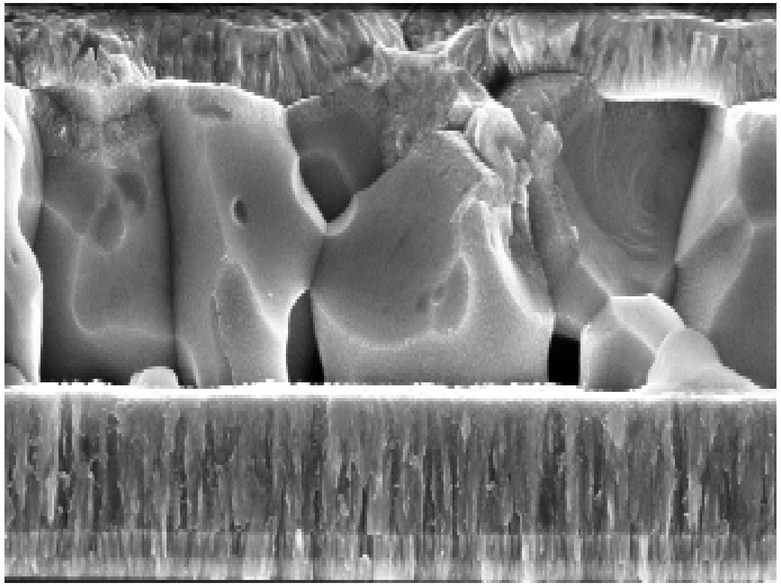
NEXCIS technological issues

- To increase PV conversion efficiency to 12 %
- Control reproducibility process
- Scale-up to 30x60 and 60x120 cm² modules
- To develop a non glass light module (metallic substrate & polymer encapsulation)

Roadmap of glass & metal CISEL™ modules



CISEL^{TM}



A Mo layer is deposited

An CuInSe2 layer is grown.

- ***Cu/In ratio will play on Eg and electrical properties***
- ***Layer homogeneity is a key point.***

Electrodeposited $CuInSe_2$ ***is sulphurized under annealing,*** $CuIn(S,Se)_2$***.***

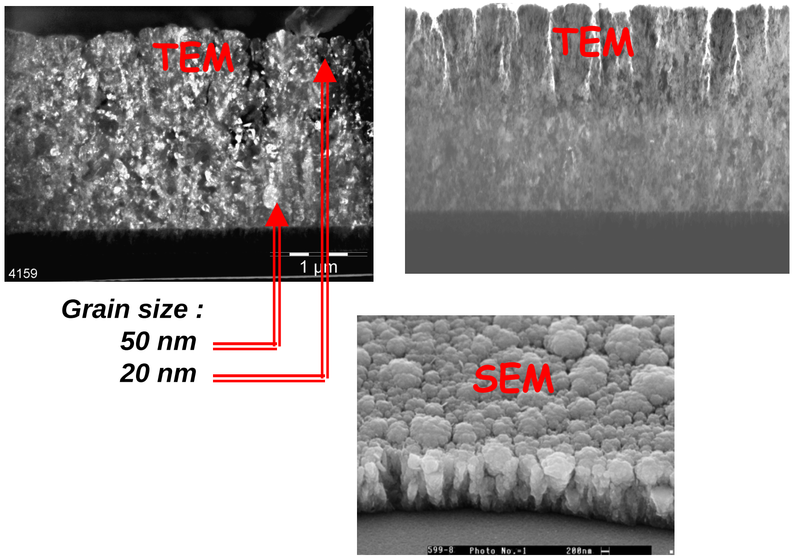
- ***Crystallization***
- ***S content.***

Important. $Mo(S,Se)_2$ ***layer formed.***

CdS buffer deposition.

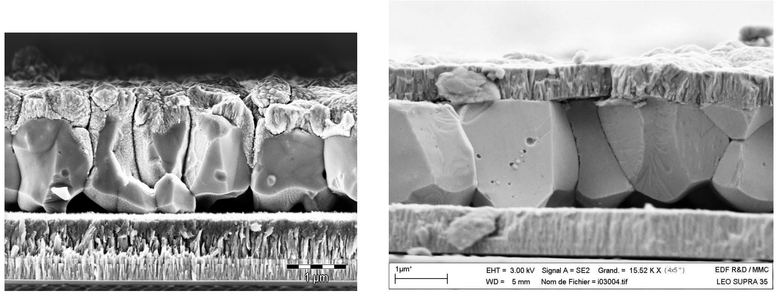
TCO sputtered.

Characterization of the CIS film, before and after annealing



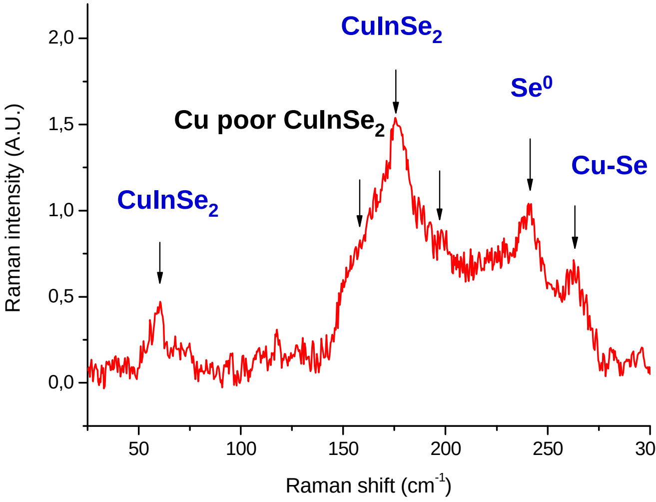
Grain size :
50 nm
20 nm

ED precursor before annealing

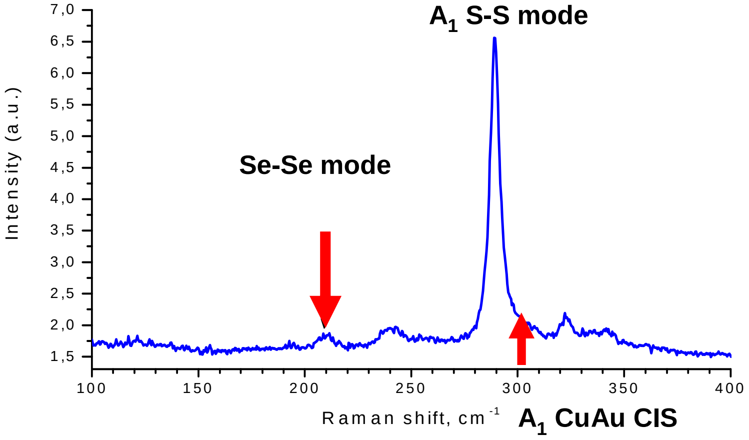


ED precursor after annealing (absorber)

- **ED phases :**



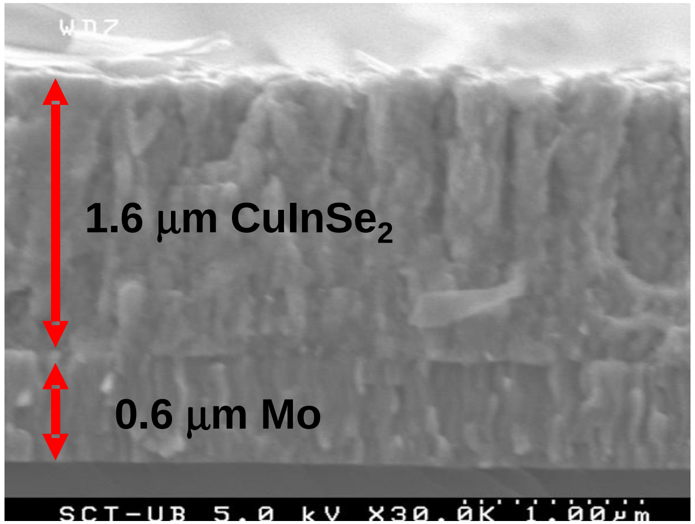
- **Absorber phases :**



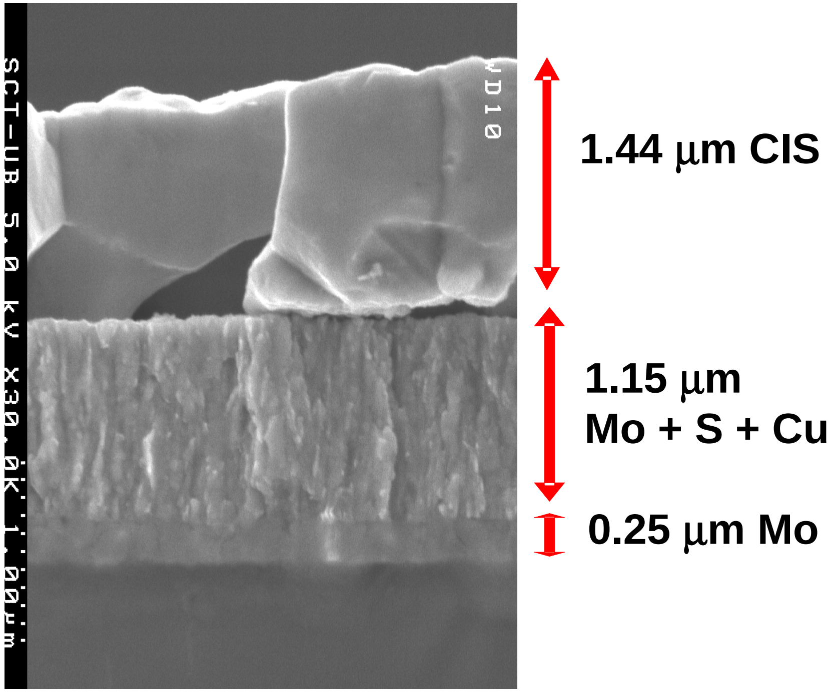
**** A. Pérez-Rodríguez et al, EME (University of Barcelona) within LARCIS project***

Annealed samples

RTA annealing in S ambient: S- rich $CuIn(S,Se)_2$ polycrystalline layers



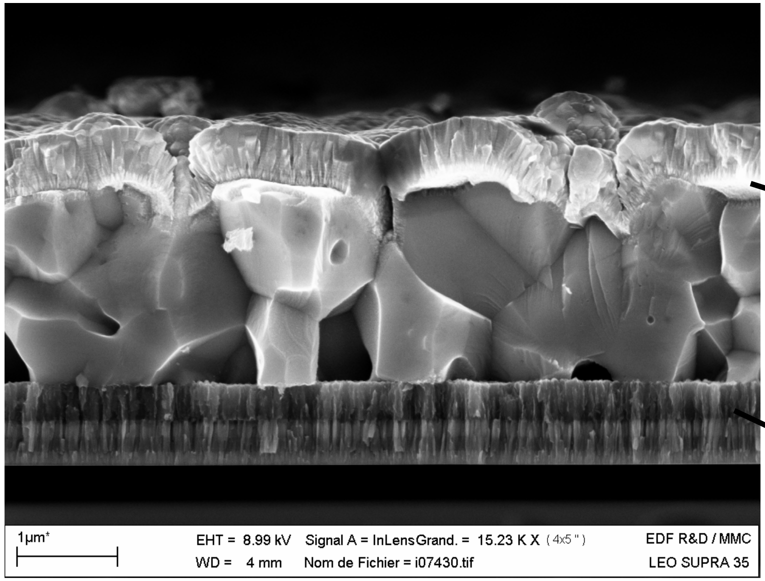
as-grown

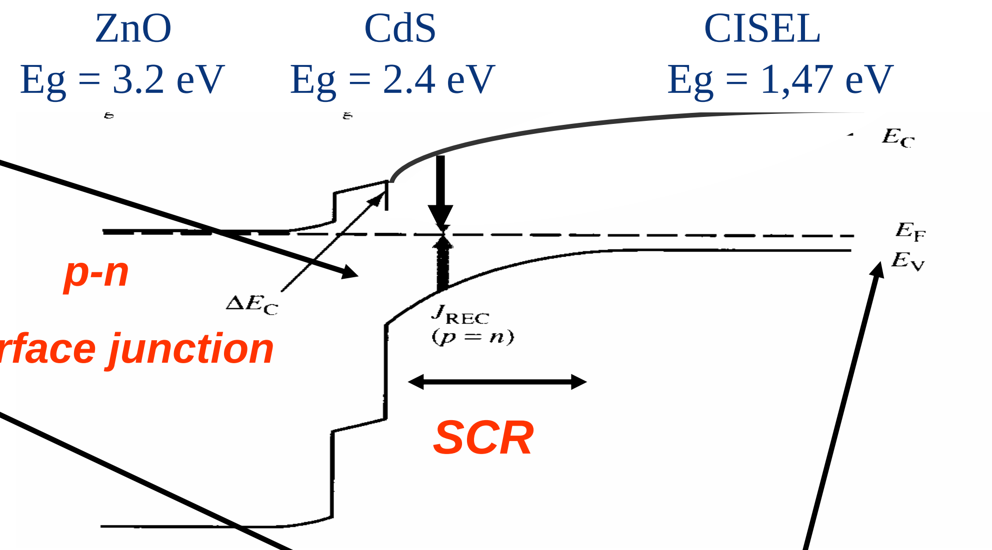


RTP annealed

CISEL cells

Up to six interfaces, glass, Mo, Mo(S,Se)$_2$, CIS, CdS, i:ZnO, ZnO:Al.





p-n

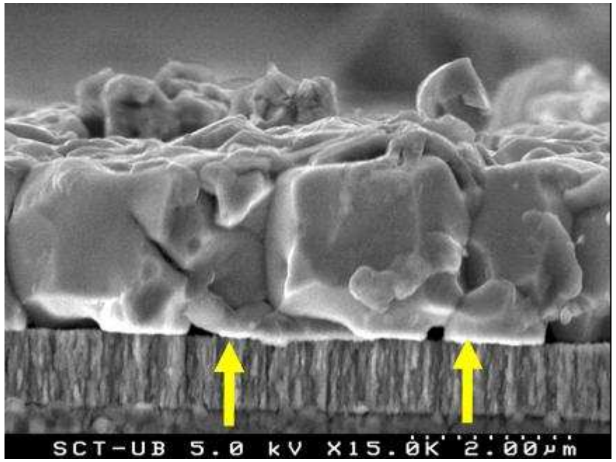
Interface junction

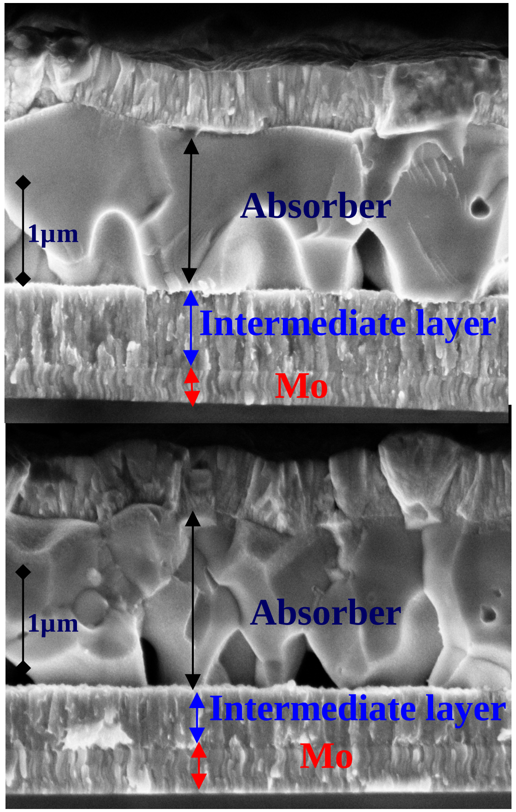
SCR

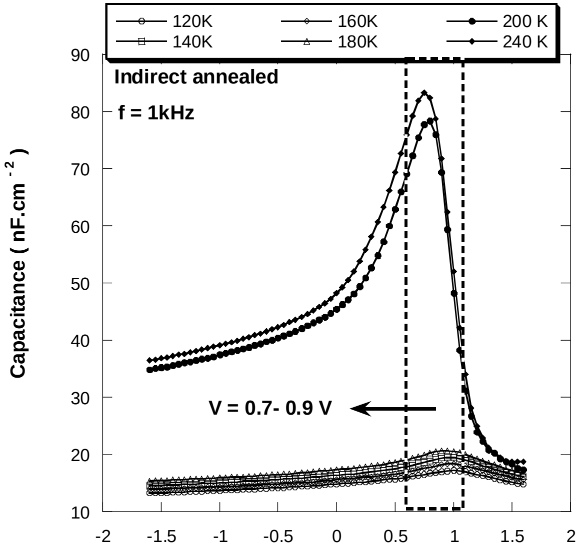
Back contact

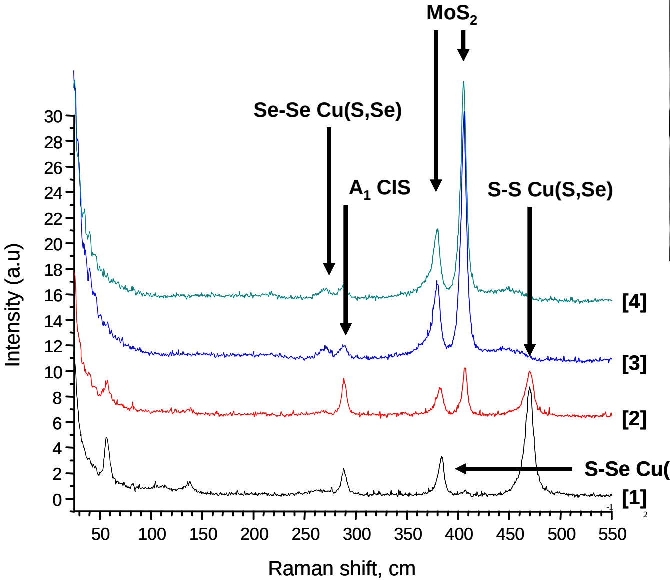
- Each Interface influence is different.
- MoSe$_2$/CISand CdS/CIS interfaces critically control the electronic transport.
- Charge carriers are generated in absorber layer, thus electronic transport does principally consist in extraction carriers and their collection to front and rear electrodes before back recombination.
-Limited, by the absorber bulk quality, and electronic quality of the absorber related interfaces.
- After charge separation at p-n junction, recombination currents will dominate the transport, relaxing the impact of other interfaces.

Particular case of study: differences in annealing procedure

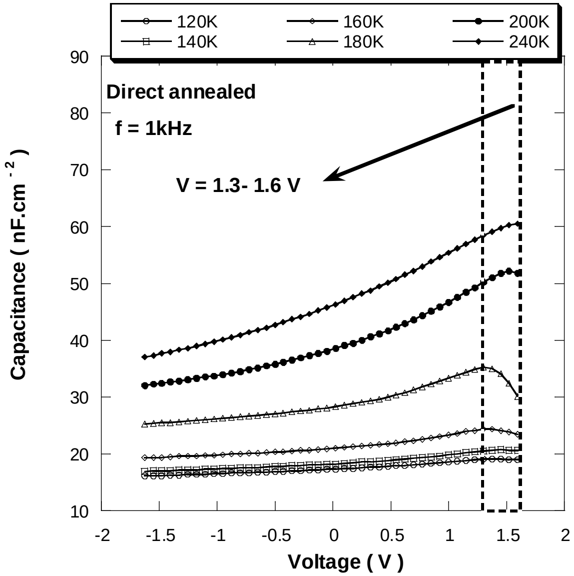








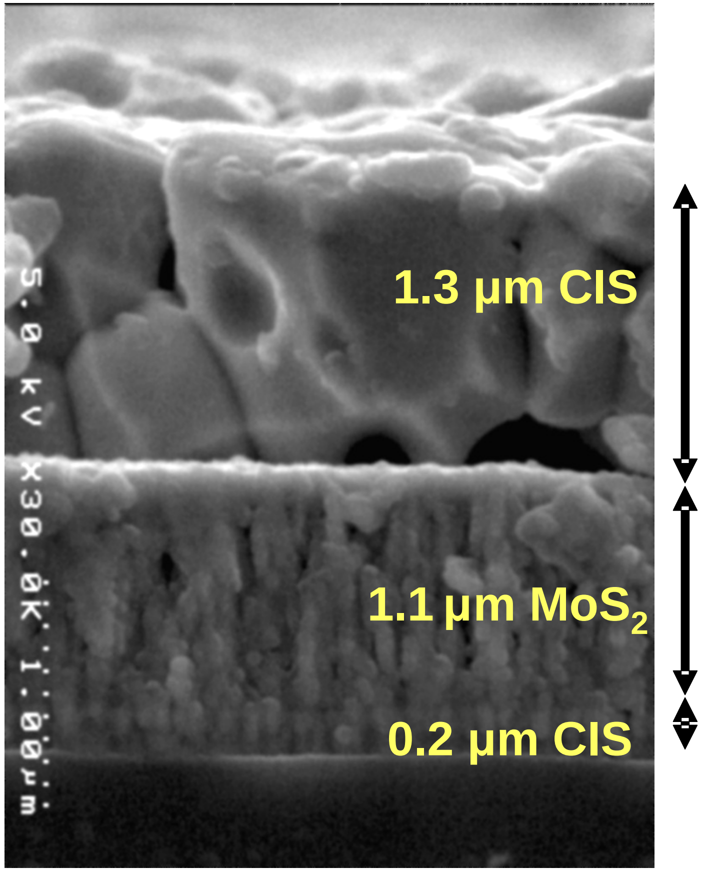
In addition, the position of the maximum is in the range of 0.7-0.9V for the indirect RTP absorber devices and between 1.3V and 1.6V for the direct RTP, indicating that the energy barrier high depend on the RTP process. This energy barrier is smaller for the indirect RTP device



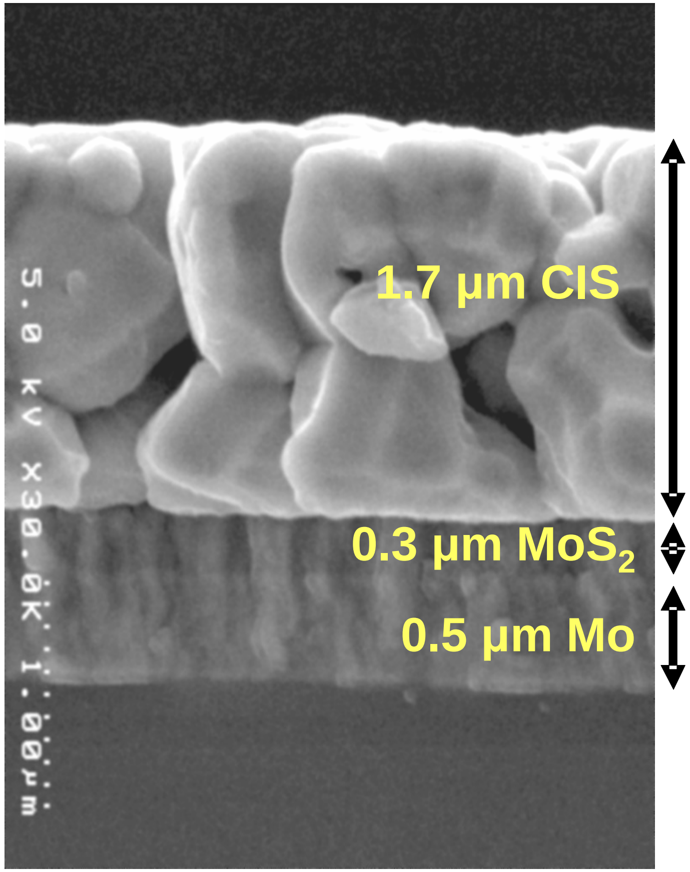
Energie barrier: Annealing temperature

Cross-section SEM: similar changes in thicknesses of CIS/MoS2/Mo

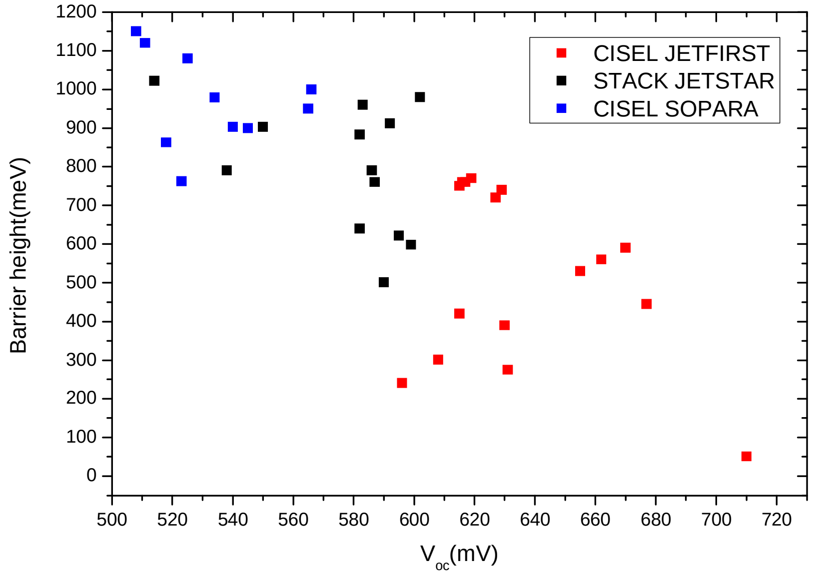
680º C

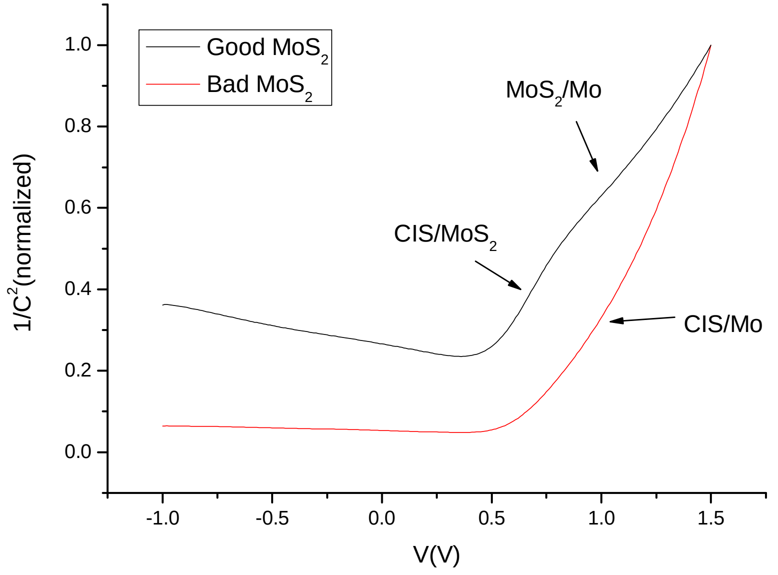


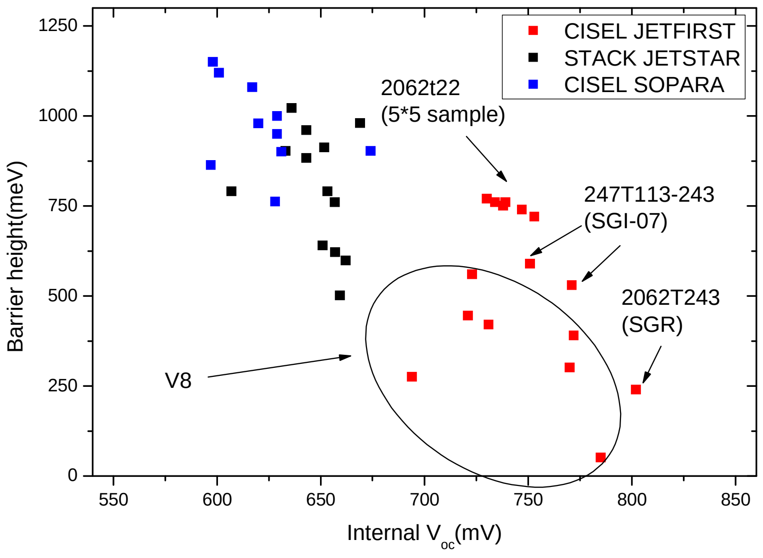
550º C



Energy barrier: annealing conditions



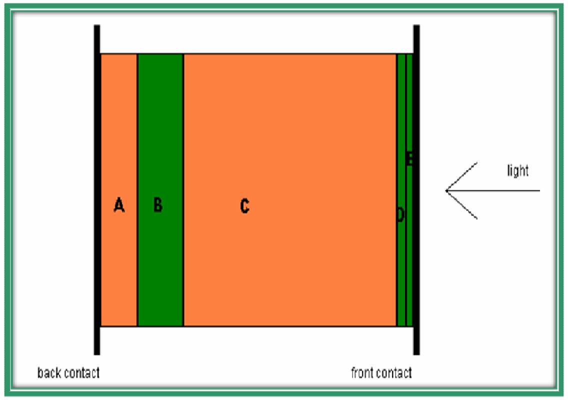




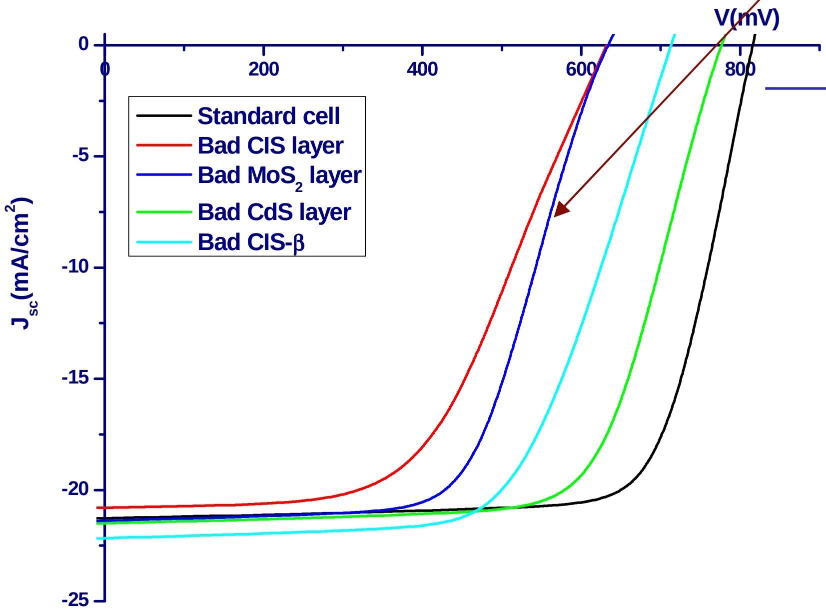
Problem in CIS/MoS$_2$ interface?

Influence of MoS_2 conductivity in cell performance (simulations)

SCAPS



	V_{oc}(mV)	J_{sc}(mA/cm^2)	FF(%)	Eff(%)
Standard cell (Theory, no defects)	816	21.261	75.17	13.04
Bad CIS	632	20.788	55.14	7.24
Bad MoS_2	633	21.378	64.06	8.66
Bad CdS	776	21.485	69.88	11.65
Bad CIS-β	713	22.164	63.31	10.01



→Small differences on Jsc

→ Problems involving the back region give smaller values of Voc

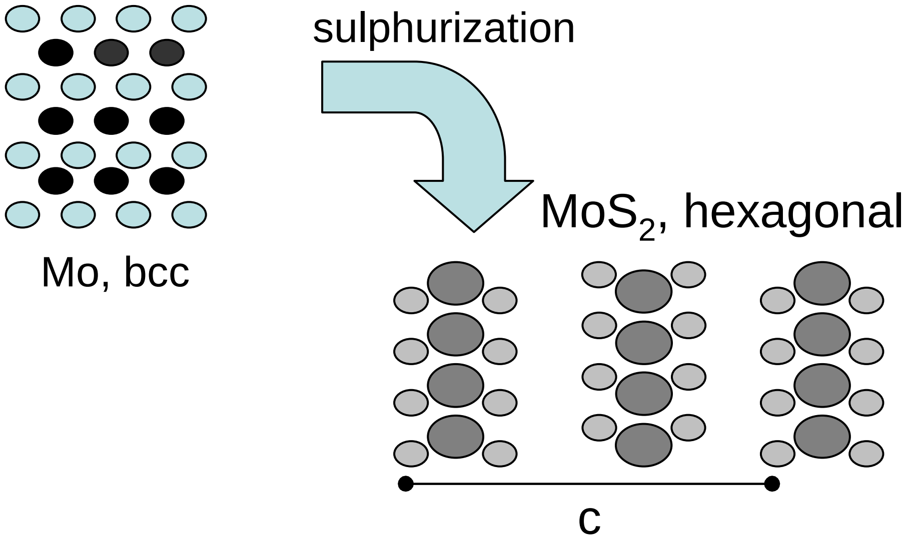
→ A bad doping density on the CIS layer leads to the biggest losses (up to 22.5%)

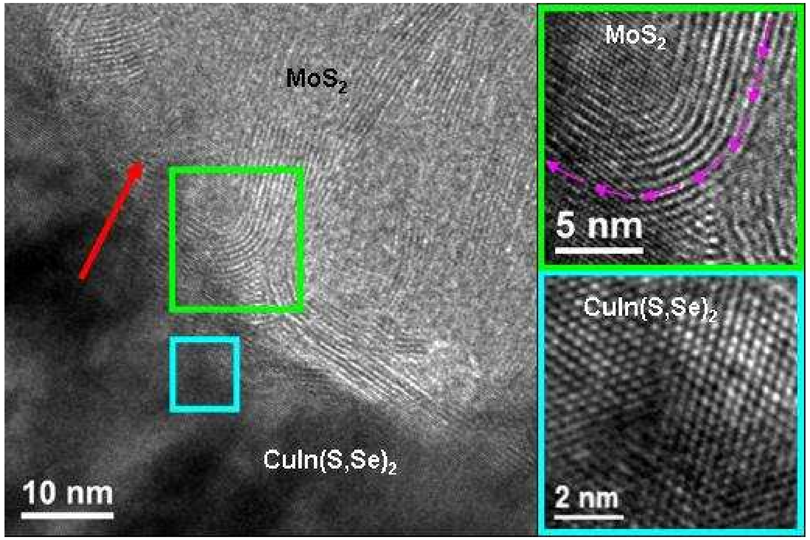
→ Also the barrier created on the back contact by the MoS2 layer gives important losses (22.4%)

→ CIS-β layer gives smaller losses on Voc (12.6%) but the FF is more degradated than in the other cases

→ The p-i-n structure created by the CdS affects minimally tu the Voc value

MoS_2 key layer for electrical transport and mechanical stability





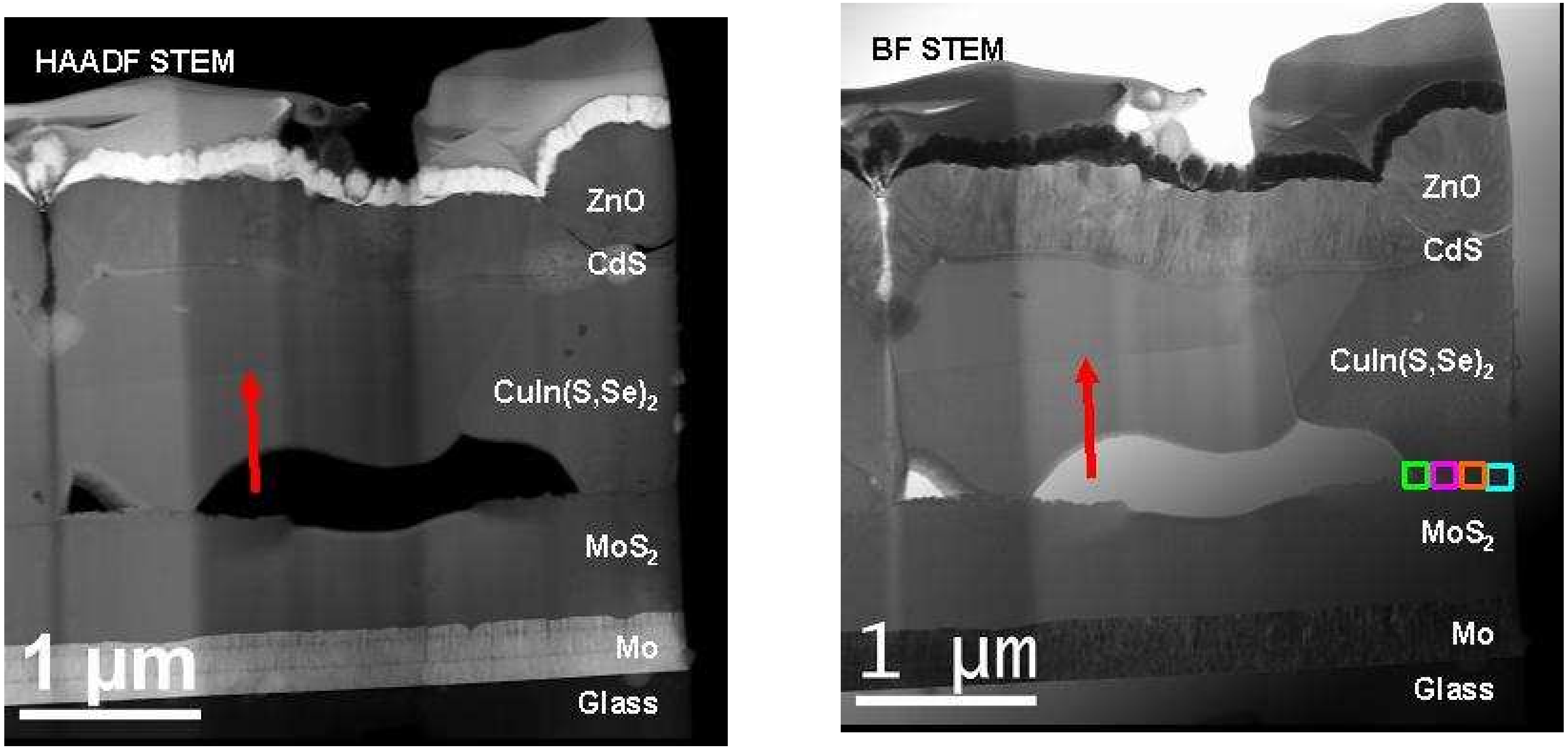
- MoS_2 c- axis orientation influences the growth kinetic, and strongly affects mechanical and electrical properties.

-Along c-axis, Van der Wal bondings between Se-Mo-Se sheets
-Perpendicular to c-axis, bonding is covalent.

} Adhesion deteriorates when MoS2 forms with c-axis in average perpendicular to the Mo surface

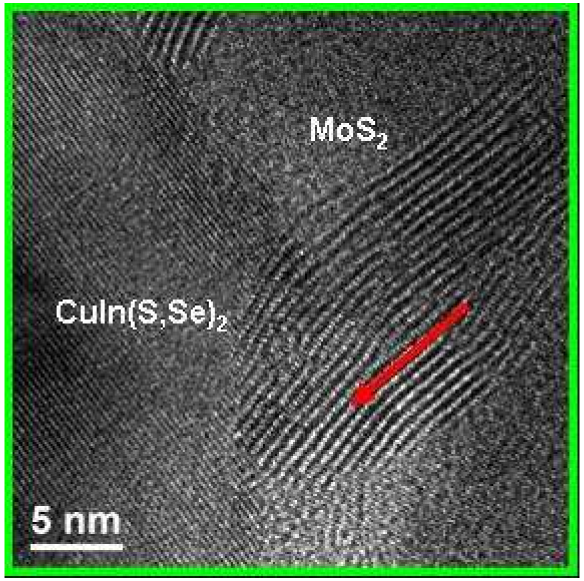
-Moreover conductivity perpendicular to the c-axis is larger by two orders of magnitude than parallel to the c-axis

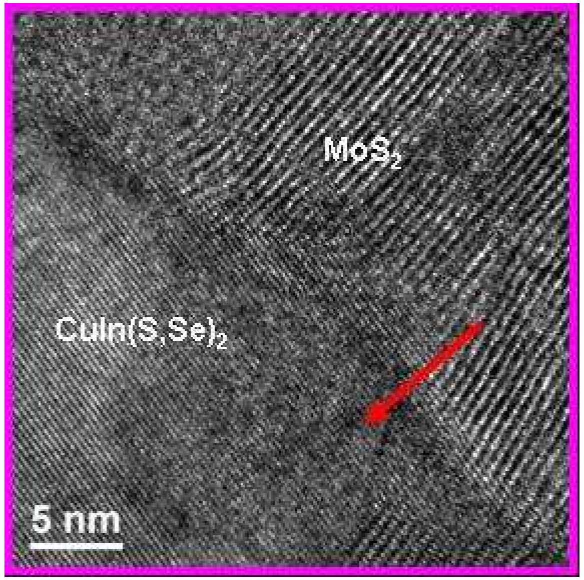
MoS_2 in CISEL^{TM} cells. No detected conductivity problem samples

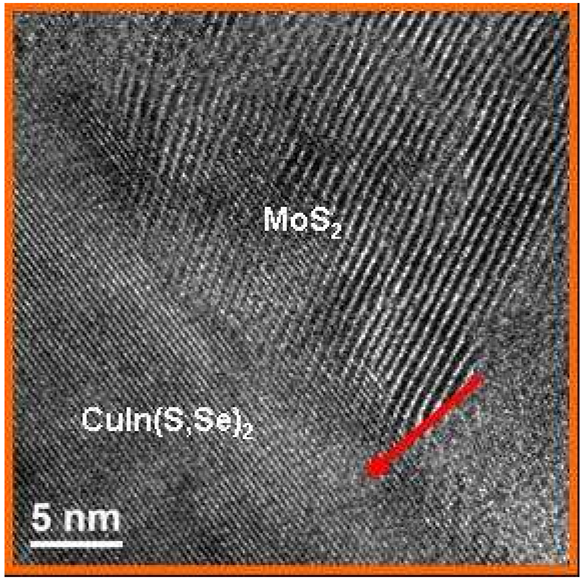


HAADF and BF STEM micrographs obtained on the sample prepared by FIB. HAADF or Z-contrast shows the compositional variations, while BF-STEM enhances the polycrystalline structure of the CuIn(S,Se)$_2$ layer. Red arrows indicate the direction perpendicular to the substrate plane. Thickness of the MoS_2 layer oscillates from 520 to 740 nm.

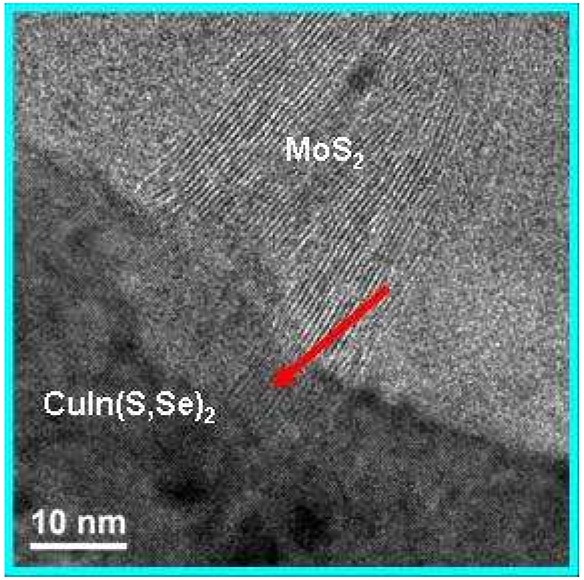
MoS_2 in CISEL^{TM} cells. No detected conductivity problem samples.



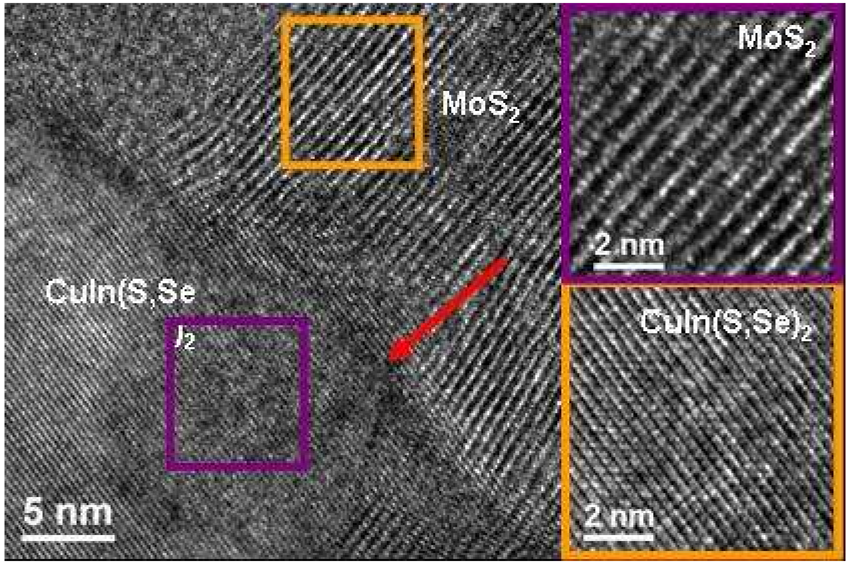


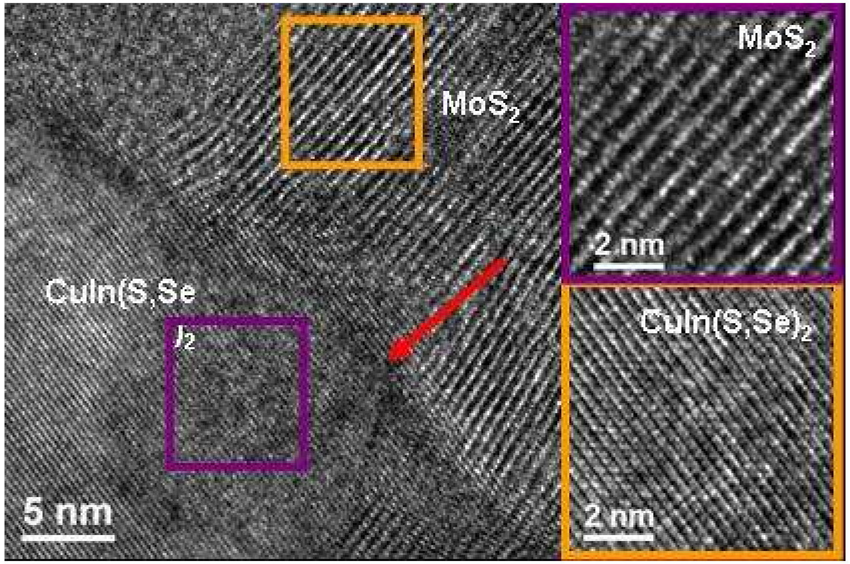


In all HRTEM images, red arrow indicates the direction perpendicular to the substrate plane. MoS_2 c-axis is found in all cases parallel to the substrate plane, thus favouring S in-diffusion during sulphurisation



MoS_2 in CISEL^{TM} cells. No detected conductivity problem samples.

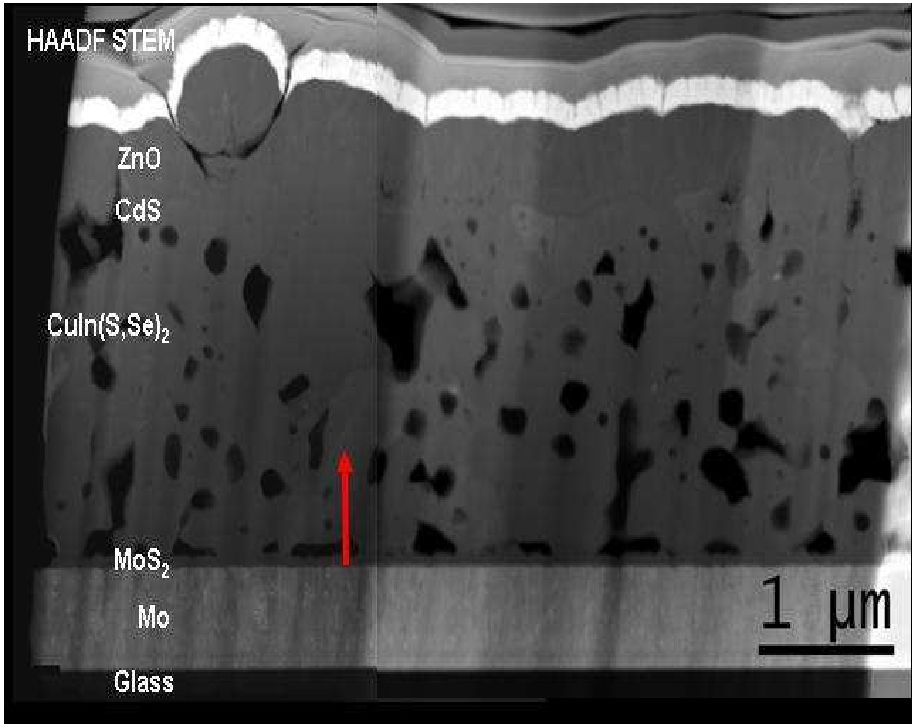


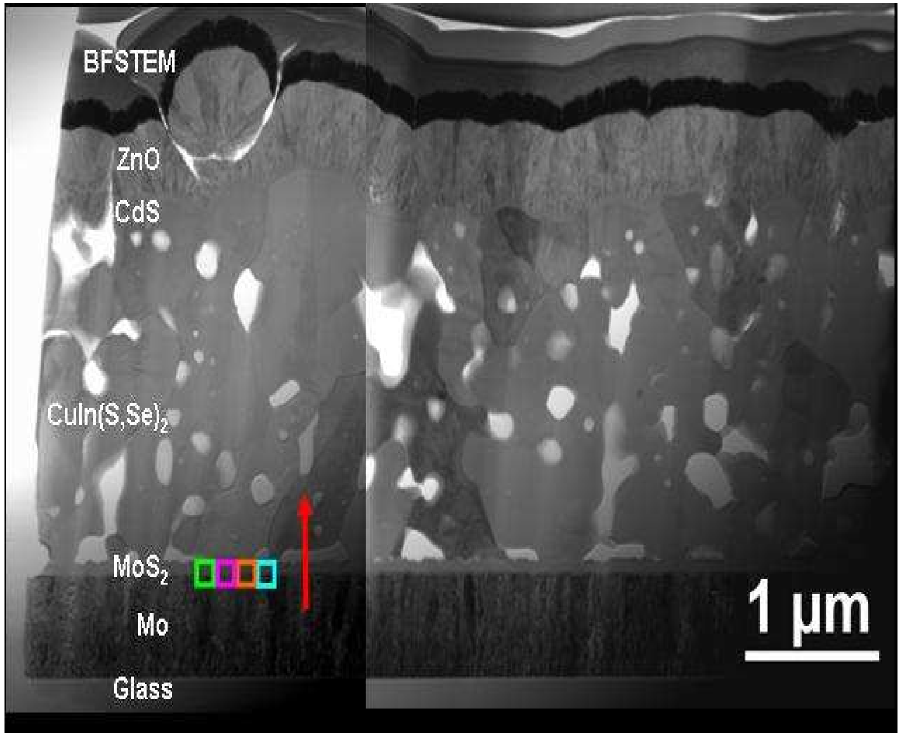


HRTEM images with magnified details on both sides of the MoS_2/CIS interface.

In cases were the measured energy barrier is low (200-400 meV) c-axis of MoS_2 in oriented parallel to the surface. And thus MoS_2 thickness is large due to S favoured diffusion.

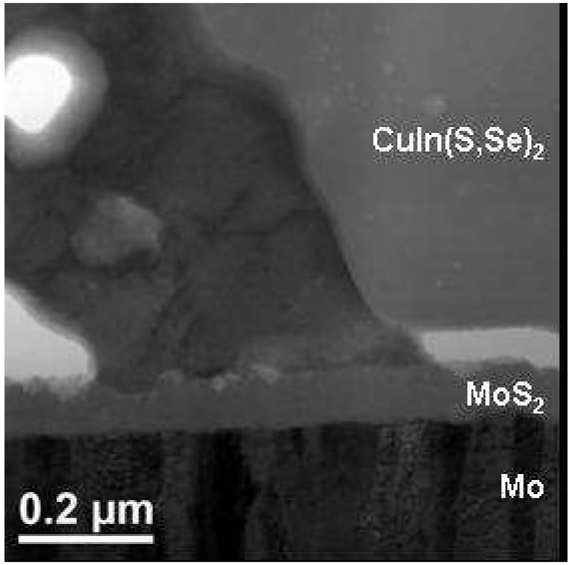
MoS$_2$ in CISEL^{TM} cells. Detected conductivity problem samples.

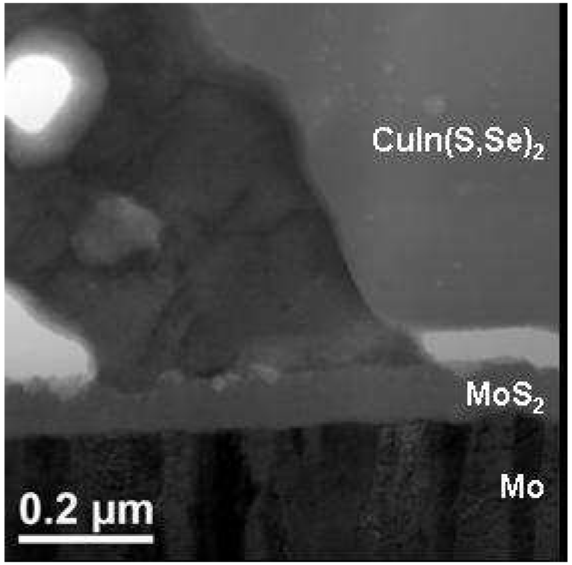




HAADF and BF STEM micrographs obtained on the sample prepared by FIB. HAADF or Z-contrast shows the compositional variations, while BF-STEM enhances the polycrystalline structure of the CuIn(S,Se)$_2$ layer. Red arrows indicate the direction perpendicular to the substrate plane. Thickness of MoS$_2$ layer oscillates from 50 to 80 nm (10 times thinner than previous sample)

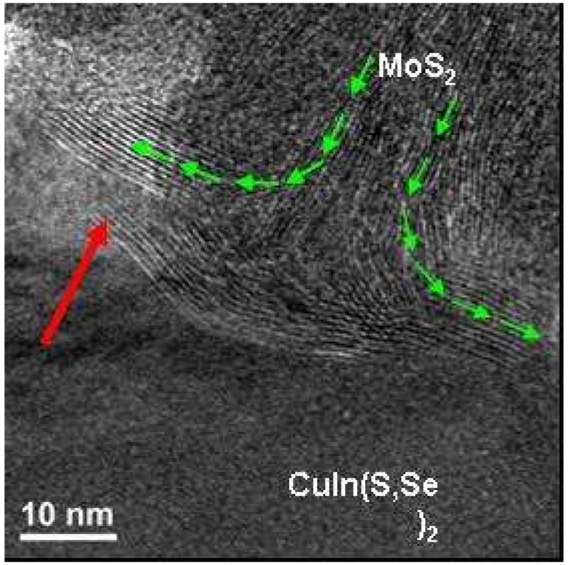
MoS_2 in CISEL™ cells. Detected conductivity problem samples.

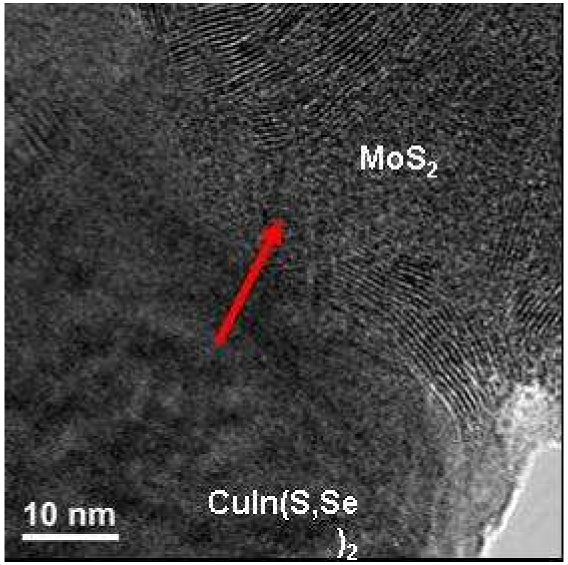




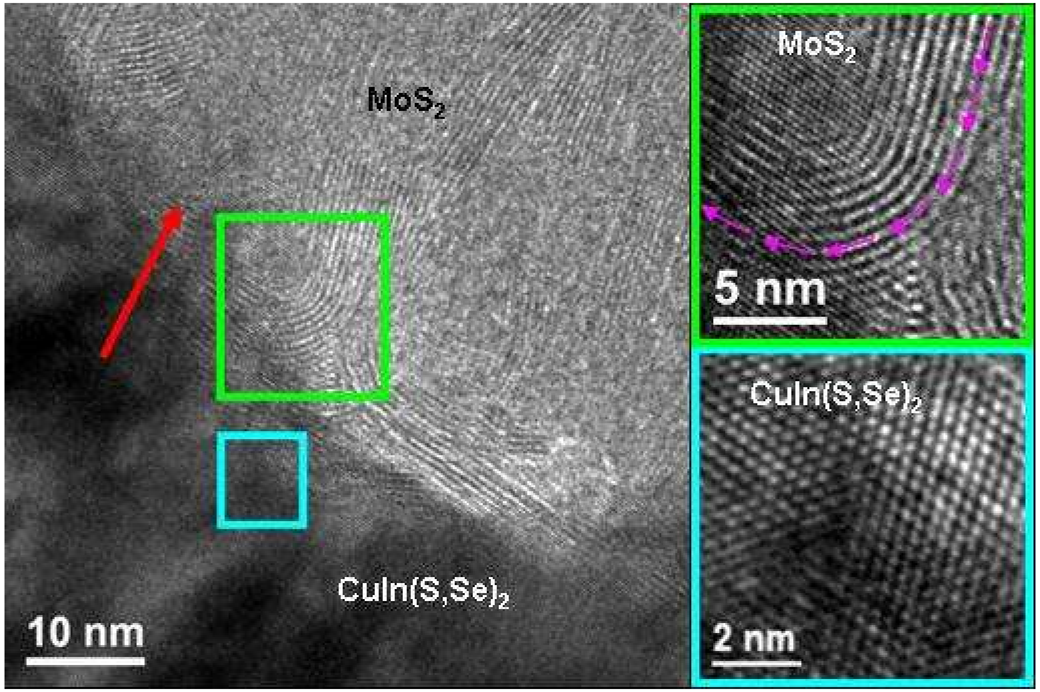
STEM micrographs suggest CIS polycrystalline layer with higher porosity

MoS_2 c-axis turn from parallel to perpendicular to the substrate plane at the CIS/Mo interface





MoS_2 in CISEL^{TM} cells. Detected conductivity problem samples.



HRTEM example with magnified details on both sides of the MoS_2/CIS interface showing the curving of MoS_2 c-planes from perpendicular to parallel to the substrate plane at the CIS/Mo interface. This likely impedes S in-diffusion during sulphurisation, and limits the MoS_2 layer thickness.

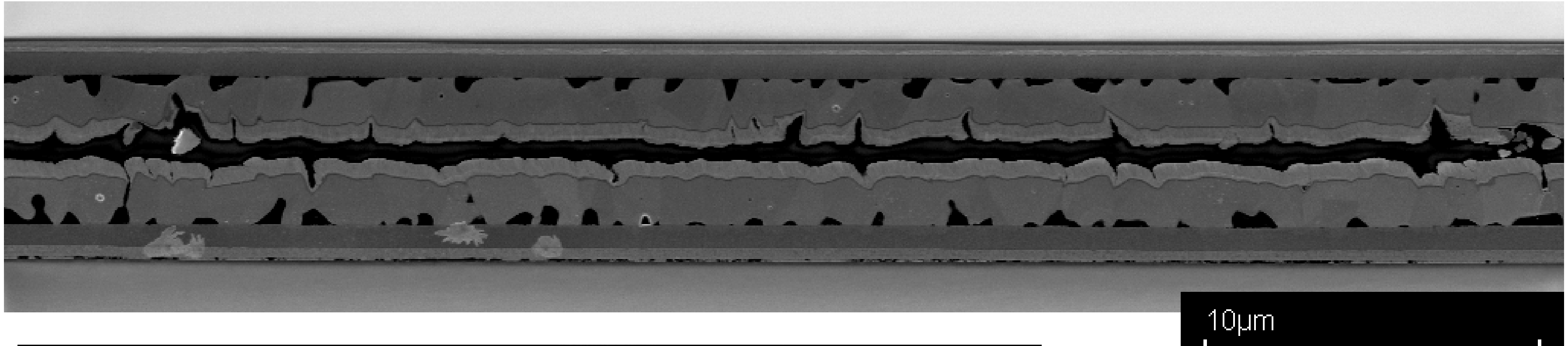
MoS_2 key layer for electrical transport and mechanical stability

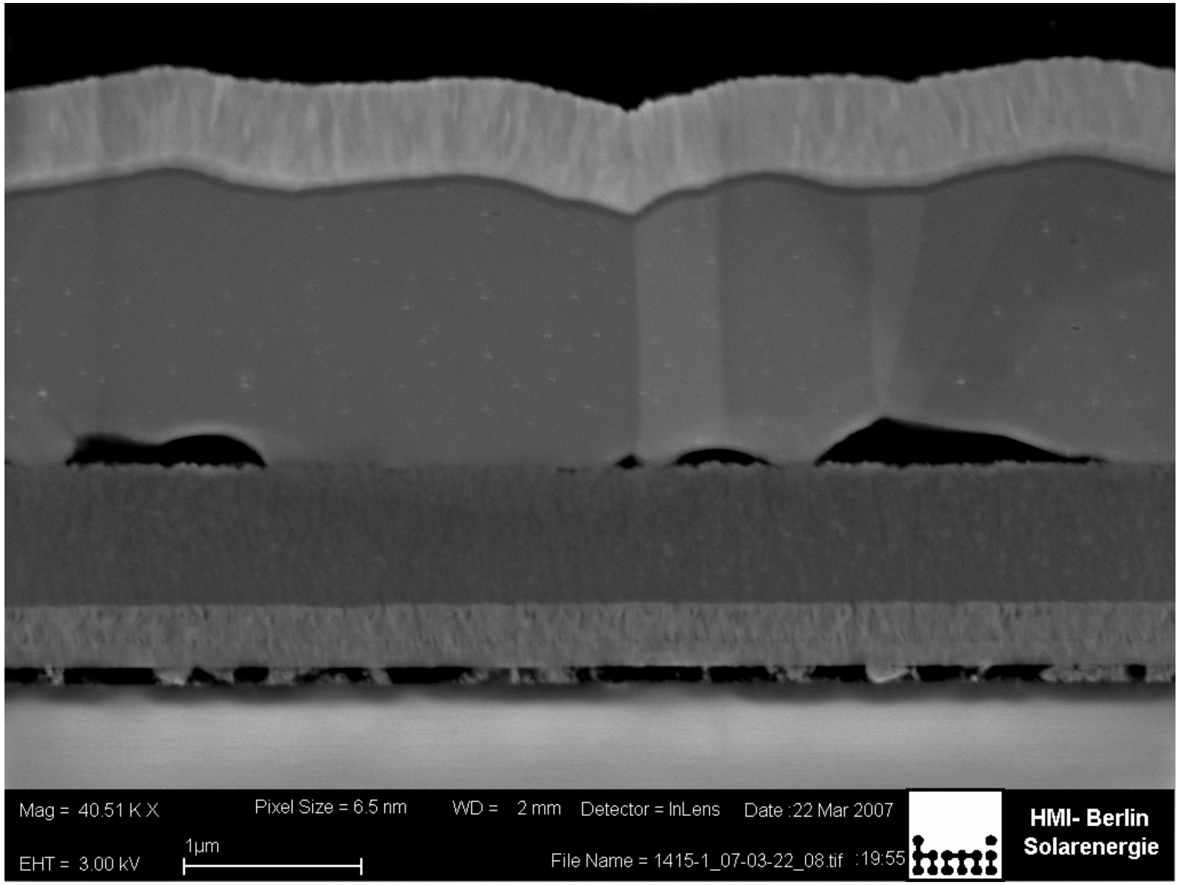
- Analitical microscopy have allows us to identify the physico-chemical origine of an opto-electronic evidence.

- When the annealing procedure favours thick MoS_2 (larger than 10-20 nm), c-axis orientation should be parallel to substrate, otherwise electrical conductivity problems arise.

- Annealing should thus favour c-axis perpendicular, and in this case small thickness (10-20 nm) are mandatory to allow for electron tunnelling.

Electron microscopy studies on $CuIn(S,Se)_2$ solar cell





Cell 1415-1, d6

ZnO
CdS

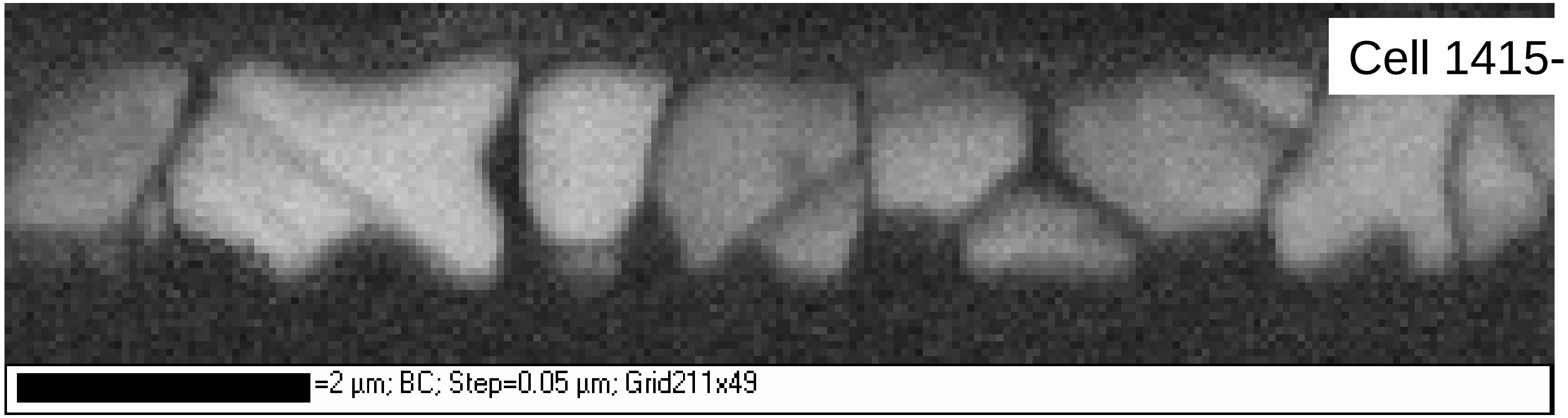
$CuIn(S,Se)_2$

$Mo(S,Se)_2$?

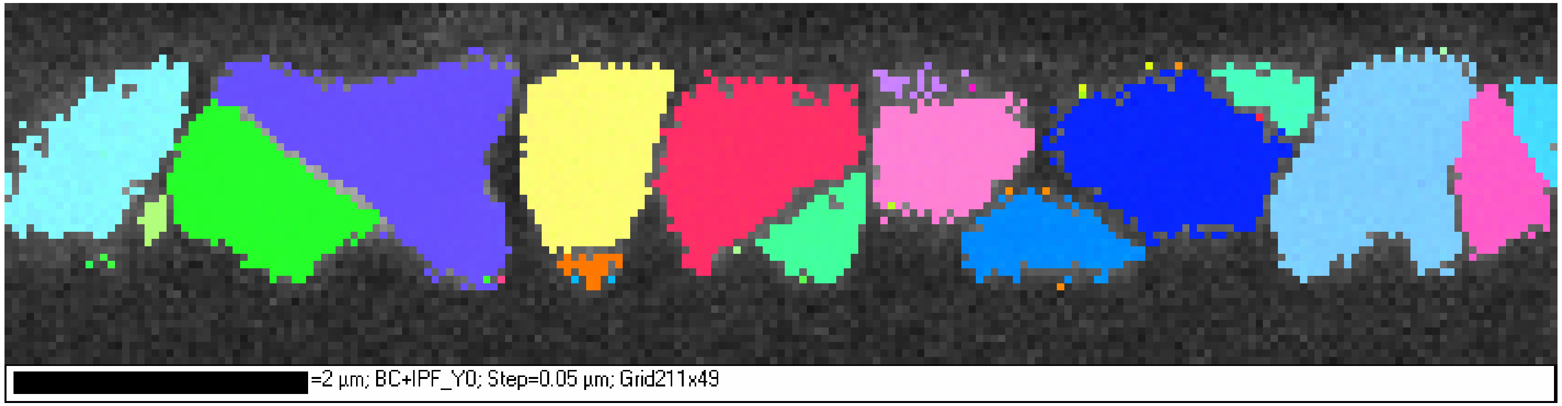
Mo

glass

Other example: electron backscatter diffraction studies

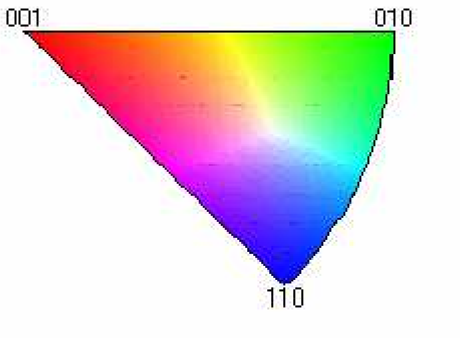


Cell 1415-1, d6



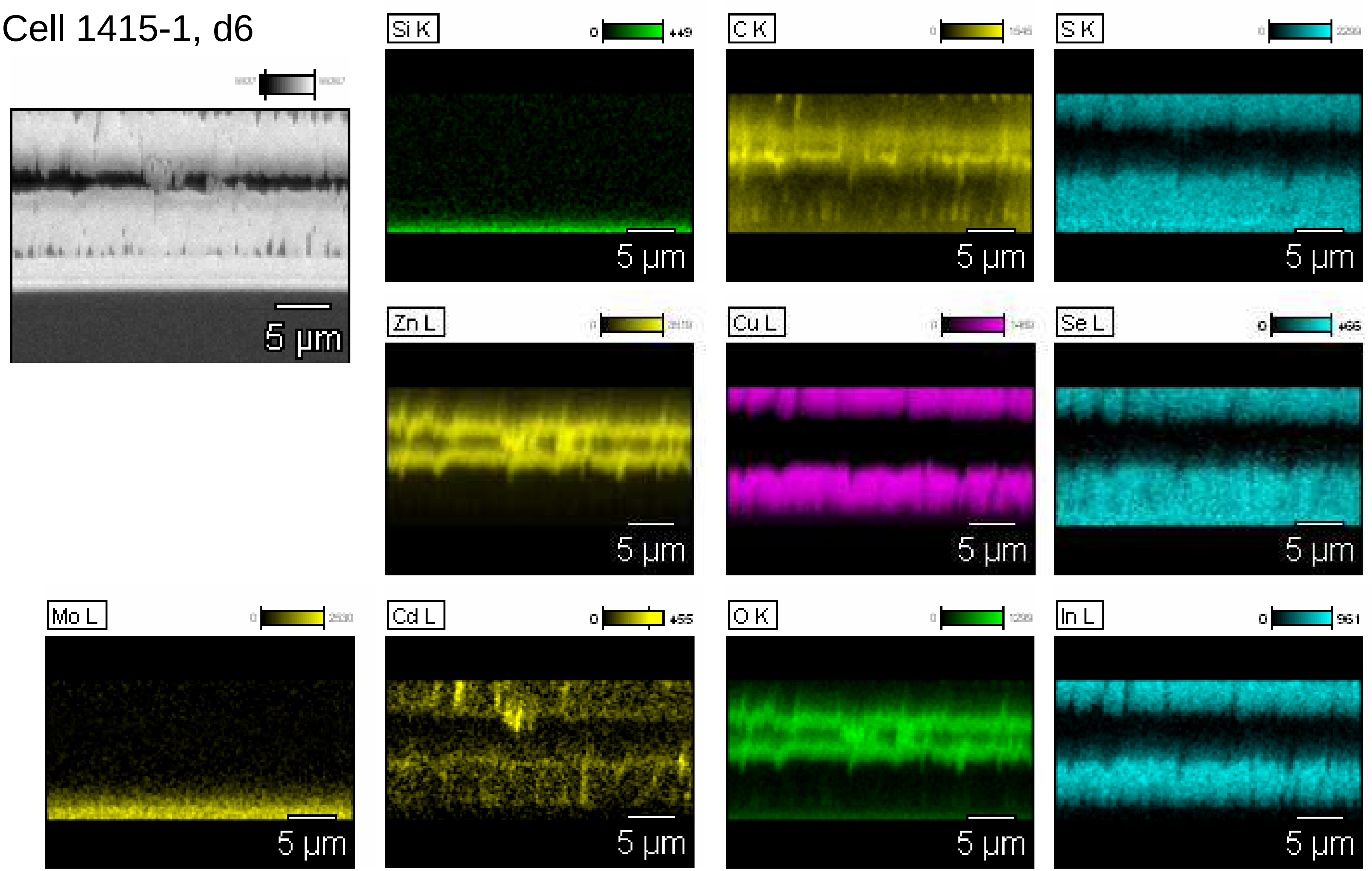
Quite large grain sizes!

Colours show that phase is identified as $CuIn(Se,S)_2$ give the local orientations of the grains.



EDX maps on cross-section samples

Cell 1415-1, d6



Data Type: Net Counts Mag: 8000 Acc. Voltage: 7.0 kV

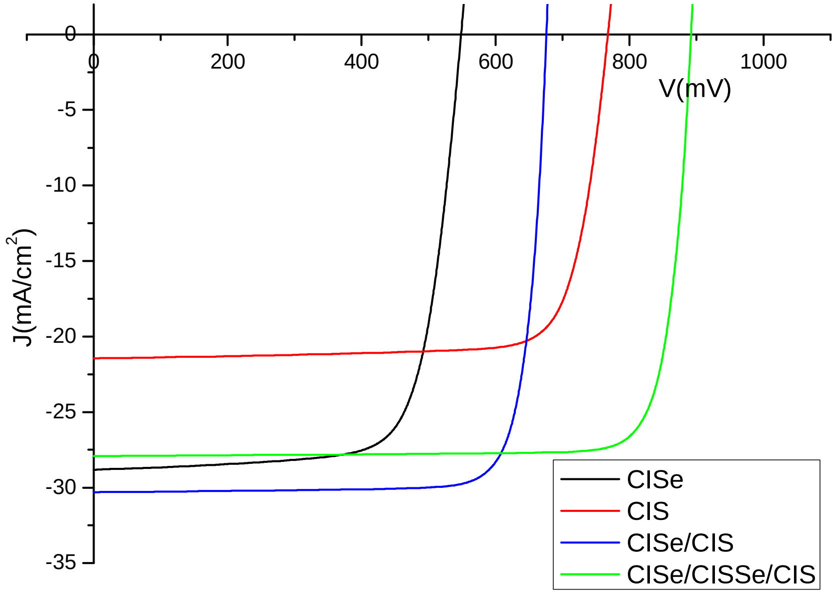
Acknowledgements

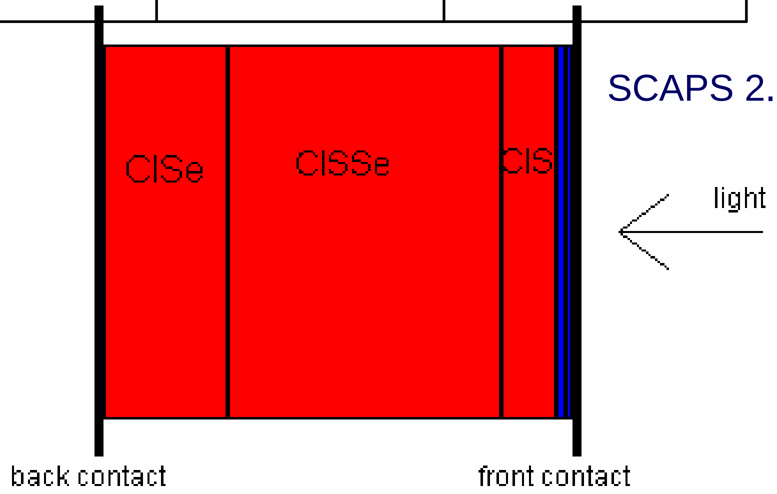
- ✓ The European Commission for funding the STREP project “LARCIS”, contract n°019757
- ✓ ADEME under GENESIS Project
- ✓ ANR (French National Research Funding Agency) under “Projet CISEL”
- ✓ All the members of IRDEP, and specially those devoted to CISEL project
- ✓ All partners and in particular: Enginyria i Materials Electronics, Barcelona University (A. Perez-Rodriguez, V. Izquierdo-Roca)

THANK YOU

Numerical simulation for graded band gap

	V_{oc} (mV)	J_{sc}(mA/cm^2)	FF(%)	Eff(%)
CISe (2µm)	**548**	**28.8**	**74.1**	**11.7**
CIS (2µm)	**768**	**21.4**	**80.2**	**13.2**
CIS/CISe (2µm+0,1µm)	**677**	**30.3**	**83.1**	**17.1**
CIS/CISSe/CISe	**893**	**27.9**	**85.6**	**21.3**



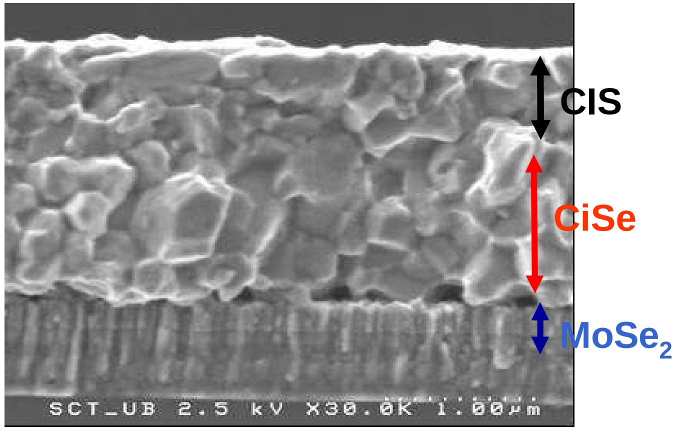


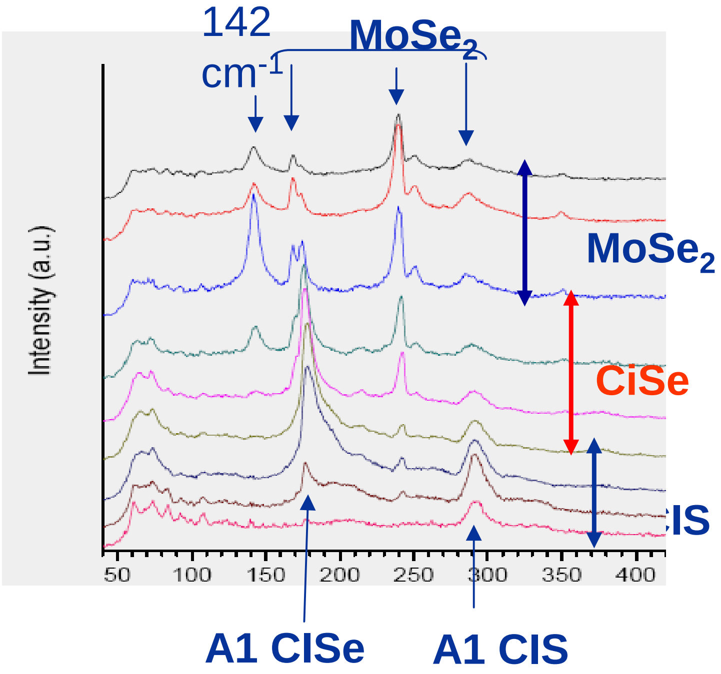
SCAPS 2.7.03

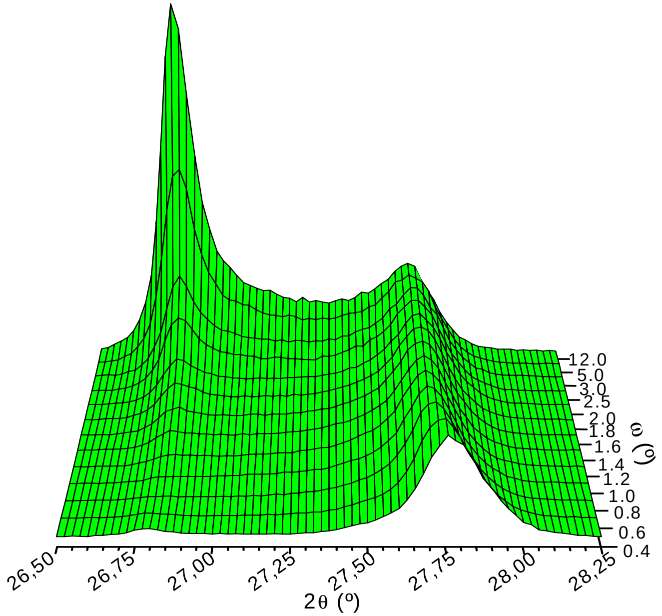
0.8 µm CISe +1.8 µm CISSe (band gap 1.23 eV)
+ 0.4 µm CIS

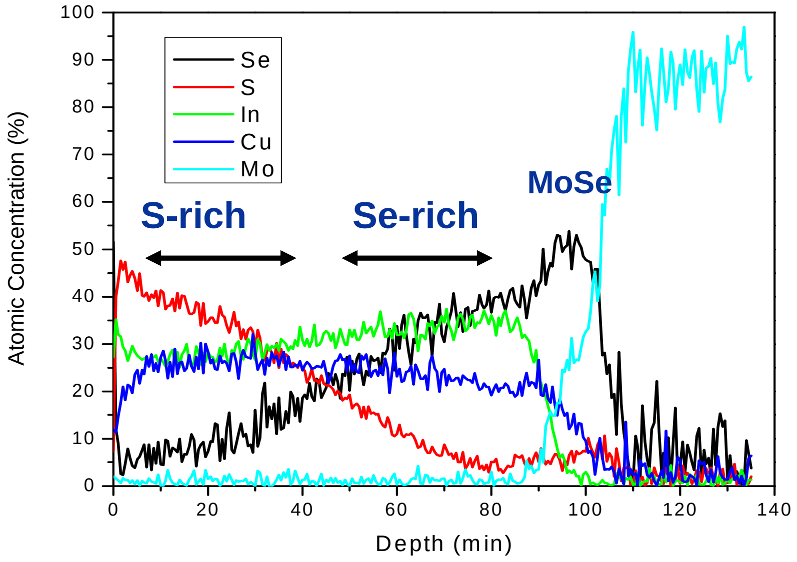
M. Burgelman, P. Nollet and S. Degrave, "Modelling polycrystalline semiconductor solar cells", Thin Solid Films 361-362 (2000), pp. 527-532

Graded material from CuInS$_2$ in surface to CuInSe$_2$ at bottom.









In collaboration with A. Pérez-Rodríguez et al,

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